Multi-Phase PWM Controller for CPU Core Power Supply

General Description

RT9245A is a multi-phase buck DC/DC controller integrated with all control functions for AMD K8 CPU or Intel® GHz CPU which is VRD10.x-compliant. The RT9245A could be operated with 2, 3 or 4 buck switching stages operating in interleaved phase set automatically. The multiphase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9245A implements both voltage and current loops to achieve good regulation, response and power stage thermal balance.

RT9245A applies the DCR sensing technology newly. The RT9245A extracts the DCR of output inductor as sense component to deliver a precise load line regulation and good thermal balance for next generation processor application.

Current sense setting, droop tuning, V_{CORE} initial offset and over current protection are independent on compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning. The DAC output of RT9245A supports AMD K8 5-bit VID and Intel® VRD10.x with 6-bit VID input, precise offset value & smooth V_{CORE} transient at VID jump. The IC monitors the V_{CORE} voltage for PGOOD and over-voltage protection. Soft-start, over-current protection and programmable under-voltage lockout are also provided to assure the safety of microprocessor and power system. The RT9245A comes to a small footprint package TSSOP-28.

Ordering Information

RT9245A □ □

- Package Type
  - C : TSSOP-28
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)

Features

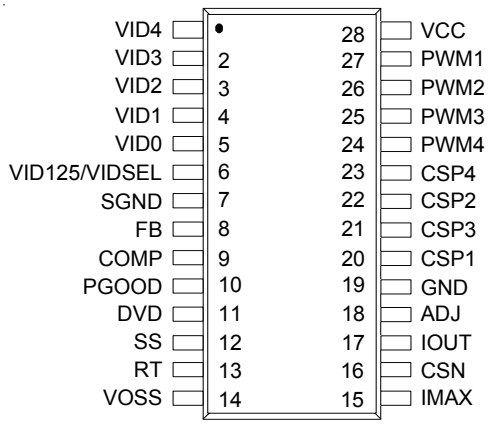
- **Multi-Phase Power Conversion with Automatic Phase Selection**
- **6-bits VRD10.x or 5-bit K8 DAC Output with Active Droop Compensation for Fast Load Transient**
- **Smooth V_{CORE} Transition at VID Jump**
- **Power Stage Thermal Balance by DCR Current Sense**
- **Hiccup Mode Over-Current Protection**
- **Programmable Switching Frequency (50kHz to 400kHz per Phase), Under-Voltage Lockout and Soft-Start**
- **High Ripple Frequency Times Channel Number**
- **28-TSSOP Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Intel® Processors Voltage Regulator : VRD10.x and AMD K8
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

Pin Configurations

(TOP VIEW)



TSSOP-28

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Typical Application Circuit

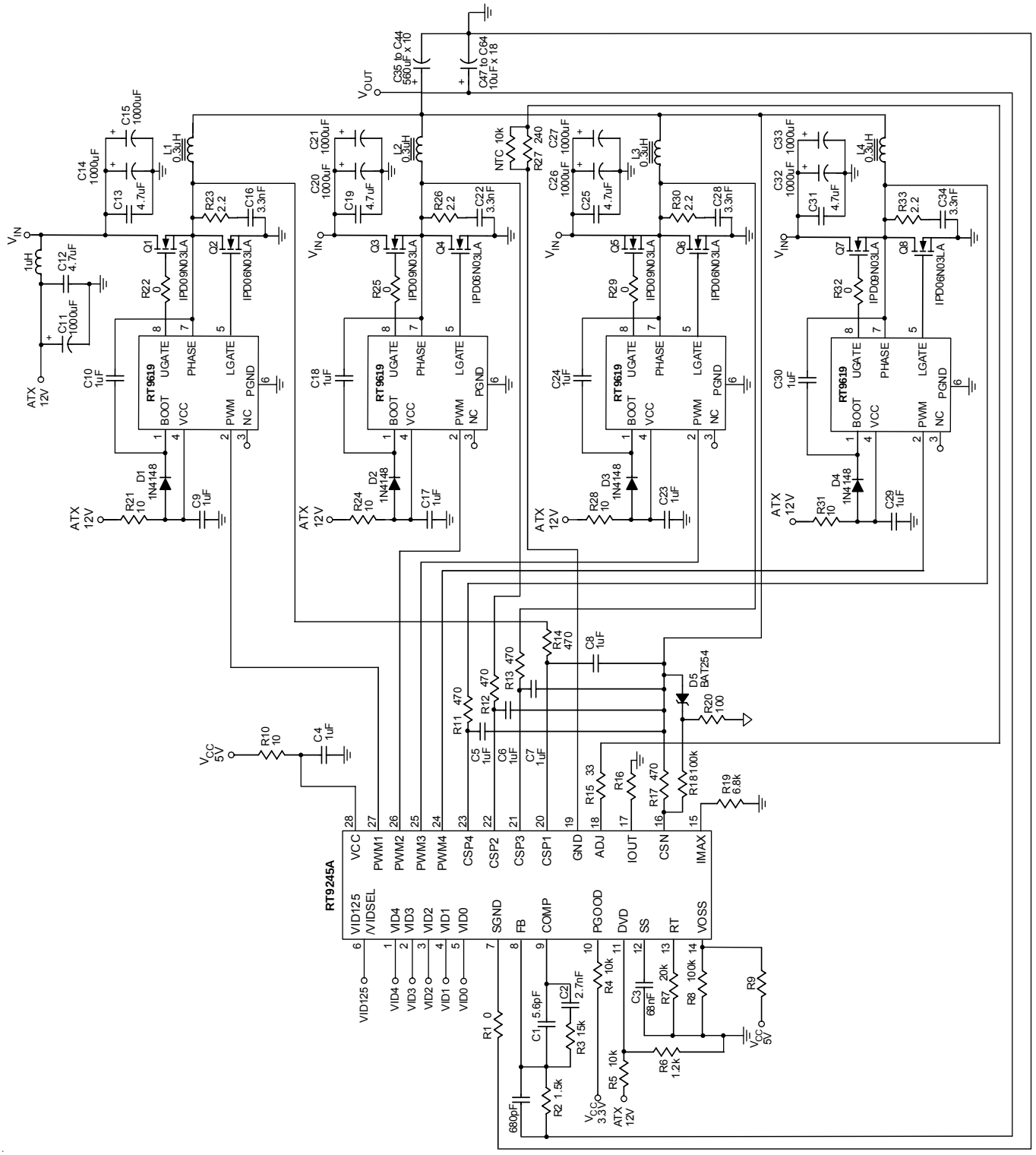


Figure A. For Intel

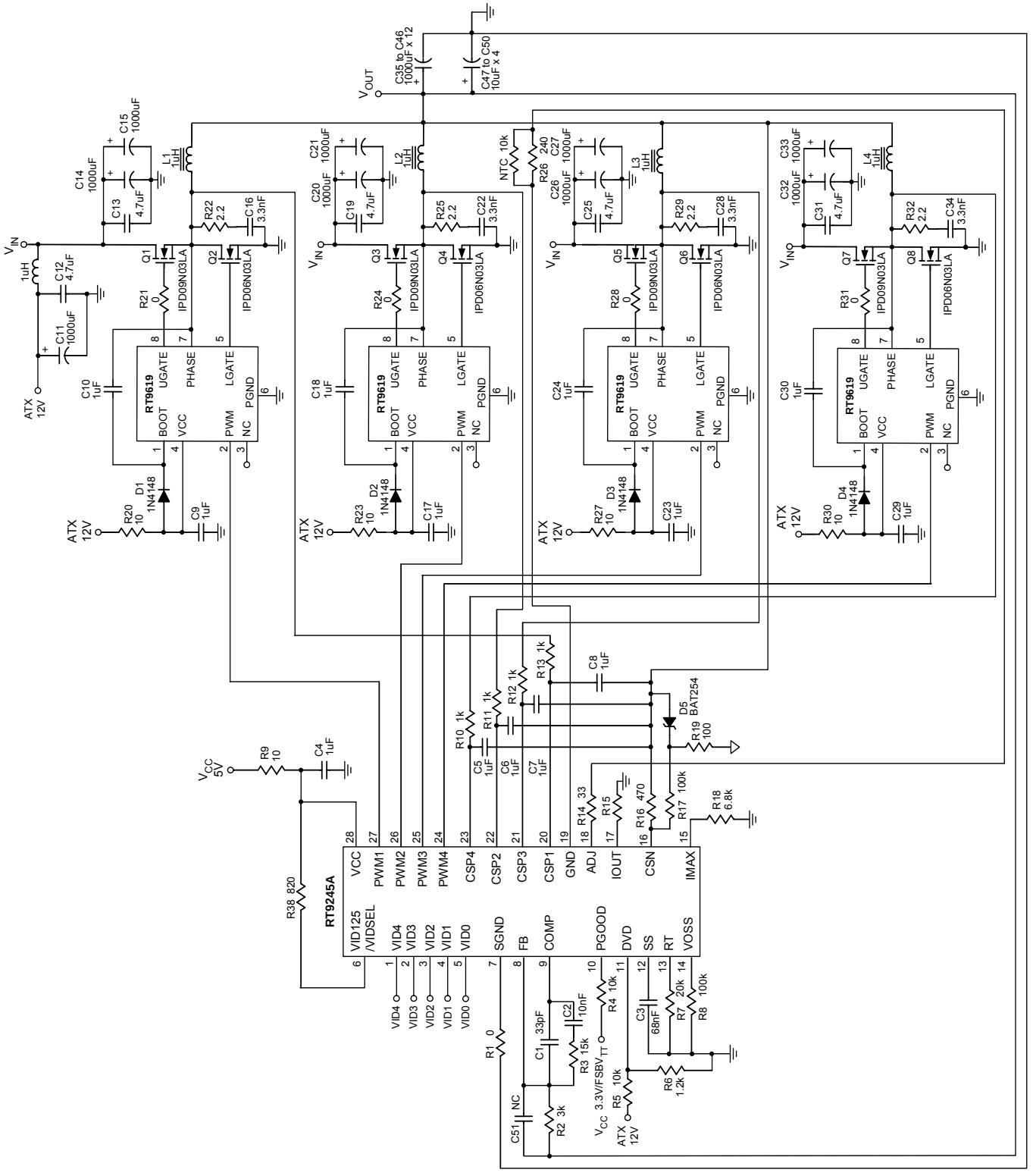


Figure B. For AMD

Functional Pin Description

VID4 (Pin 1), VID3 (Pin 2), VID2 (Pin 3), VID1 (Pin 4), VID0 (Pin 5)

DAC voltage identification inputs for VRD10.x. These pins are internally pulled to 1.2V (VRD10.x) or 2.1V (K8) if left open.

VID125/VIDSEL (Pin 6)

When this pin pull low or left pen -->VR10 VID input, pull high to 5V -->K8.

SGND (Pin 7)

V_{CORE} differential sense negative input.

FB (Pin 8)

Inverting input of the internal error amplifier.

COMP (Pin 9)

Output of the error amplifier and input of the PWM comparator.

PGOOD (Pin 10)

Power good open-drain output.

DVD (Pin 11)

Programmable power UVLO detection input. Trip threshold = 1.0V at V_{DVD} rising.

SS (Pin 12)

Connect this SS pin to GND with a capacitor to set the soft-start time interval.

RT (Pin 13)

Switching frequency setting. Connect this pin to GND with a resistor to set the frequency.

VOSS (Pin 14)

V_{CORE} initial value offset. Connect this pin to GND with a resistor to set the negative offset value. Connect this pin to VCC to set positive offset value.

IMAX (Pin 15)

Programmable over currert setting.

CSN (Pin 16)

Current sense negative input of all channels.

IOUT (Pin 17)

Output Current Indication Pin. The current through IOUT pin is proportional to the output current.

ADJ (Pin 18)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the load droop.

GND (Pin 19)

Ground for the IC.

CSP1 (Pin 20), CSP2 (Pin 22), CSP3 (Pin 21) & CSP4 (Pin 23)

Current sense positive inputs for individual converter channel current sense.

PWM1 (Pin 27), PWM2 (Pin 26), PWM3 (Pin 25) & PWM4 (Pin 24)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver. For systems which use 3 channels, connect PWM4 high. Two channel systems connect PWM3 high.

VCC (Pin 28)

IC power supply. Connect this pin to a 5V supply.

Function Block Diagram

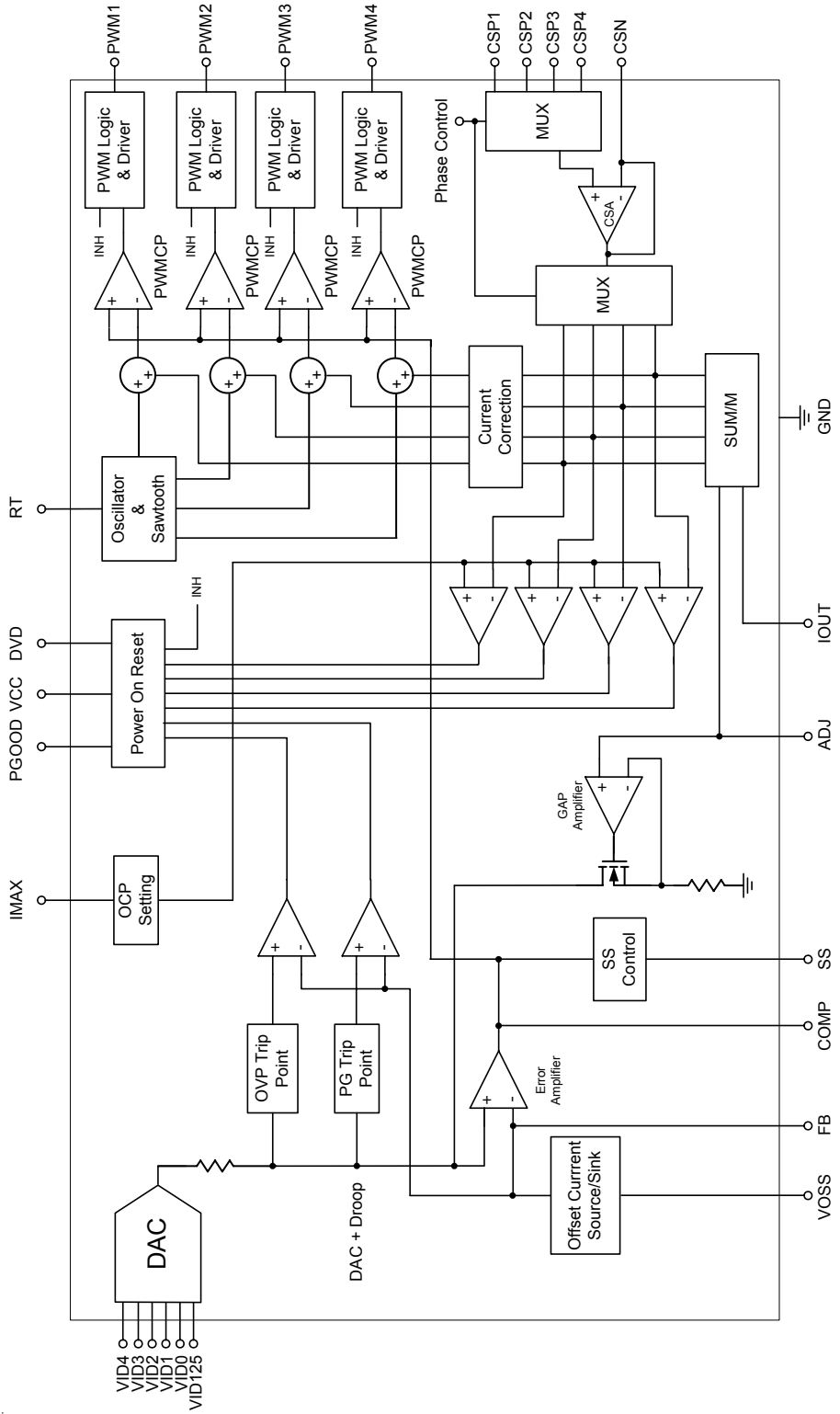


Table 1. Output Voltage Program (VRD 10.x)

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	1	1	1	X	No CPU
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.850V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.875V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.900V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.925V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.950V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.025V
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.050V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.075V
0	0	0	0	0	0	1.0875V
1	1	1	1	0	1	1.100V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.125V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.150V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.175V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.200V
1	1	0	1	0	0	1.2125V

To be continued

Table 1. Output Voltage Program (VRD 10.x)

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	0	0	1	1	1.225V
1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.250V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.275V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.300V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.325V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.350V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.375V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.400V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.425V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.450V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.475V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.500V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.525V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.550V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.575V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Note: (1) 0 : Connected to GND
(2) 1 : Open
(3) X : Don't Care

Table 2. Output Voltage Program (K8)

VID4	VID3	VID2	VID1	VID0	Nominal Output Voltage DACOUT
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.200
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

Note: (1) 0 : Connected to GND
(2) 1 : Open

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 7V
- Input, Output or I/O Voltage ---------- GND – 0.3V to V_{CC} + 0.3V
- Package Thermal Resistance
  TSSOP-28, θ_{JA} ---------- 100°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 5V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current							
Nominal Supply Current		I_{CC}	PWM 1,2,3,4 Open	--	12	16	mA
Power-On Reset							
POR Threshold		V_{CCRTH}	V_{CC} Rising	4.0	4.2	4.5	V
Hysteresis		V_{CCHYS}		0.2	0.5	--	V
V_{DVD} Threshold	Trip (Low to High)	V_{DVDTP}	Enable	0.94	1.0	1.06	V
	Hysteresis	V_{DVDHYS}		--	50	--	mV
Oscillator							
Free Running Frequency		f_{OSC}	R_{RT} = 20kΩ	170	200	230	kHz
Frequency Adjustable Range		f_{OSC_ADJ}		50	--	400	kHz
Ramp Amplitude		ΔV_{OSC}	R_{RT} = 20kΩ	--	1.9	--	V
Ramp Valley		V_{RV}		0.7	1.0	--	V
Maximum Duty of Each Channel				58	64	70	%
RT Pin Voltage		V_{RT}	R_{RT} = 20kΩ	0.9	1.0	1.1	V
Reference and DAC							
DACOUT Voltage Accuracy		ΔV_{DAC}	$V_{DAC} \geq 1V$	–1	--	+1	%
			$V_{DAC} < 1V$	–10	--	+10	mV
DAC (VID0-VID125) Input Low		V_{ILDAC}	VRD 10.x	--	--	0.4	V
			K8	--	--	0.8	V
DAC (VID0-VID125) Input High		V_{IHDAC}	VRD 10.x	0.8	--	--	V
			K8	1.2	--	--	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DAC (VID0-VID125) pull up resistor			2.5	3.5	4.5	kΩ
DAC Pull Up Voltage		VRD 10.x	--	1.2	--	V
		K8	--	2.1	--	V
VOSS Pin Voltage	V_{VOSS}	R_{VOSS} = 100kΩ	0.9	1.0	1.1	V
Error Amplifier						
DC Gain			--	60	--	dB
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR	COMP = 10pF	--	6	--	V/μs
Current Sense GM Amplifier						
CSN Full Scale Source Current	I_{ISPFSS}		100	--	--	μA
CSN Current for OCP			150	--	--	μA
Protection						
Over-Voltage Trip (V_{FB} – V_{DAC})	Δ_{OVT}	R_{ADJ} = 0Ω	320	400	450	mV
IMAX Voltage	V_{IMAX}	R_{IMAX} = 20kΩ	0.9	1.0	1.1	V
Power Good						
Output Low Voltage	V_{PGOODL}	I_{PGOOD} = 4mA	--	--	0.2	V

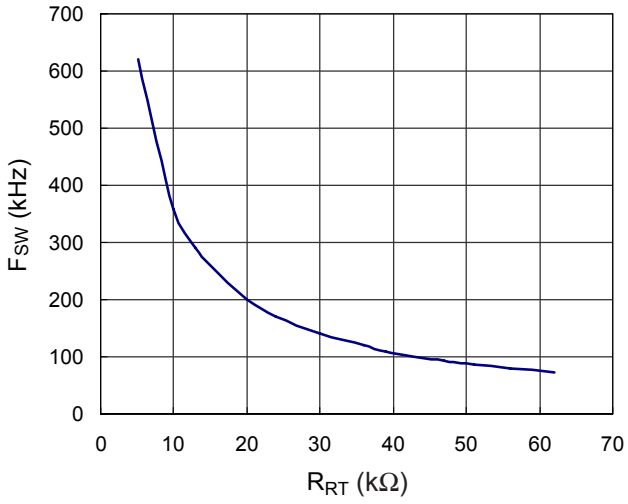
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

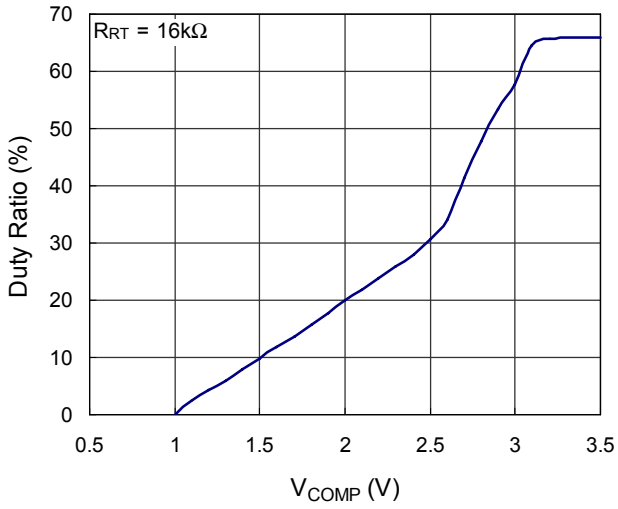
Note 3. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

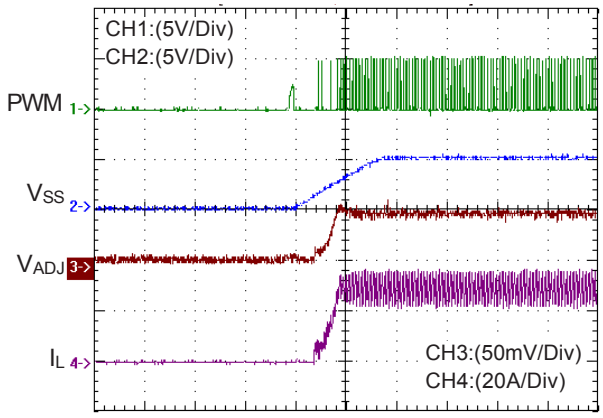
Adjustable Frequency



PWM vs. V_{COMP}

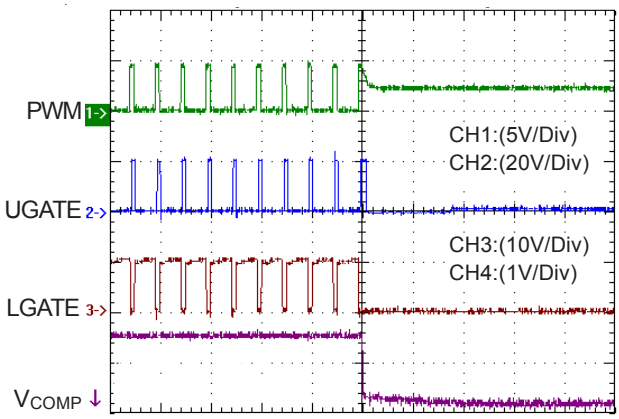


Relationship Between Inductor Current and V_{ADJ}



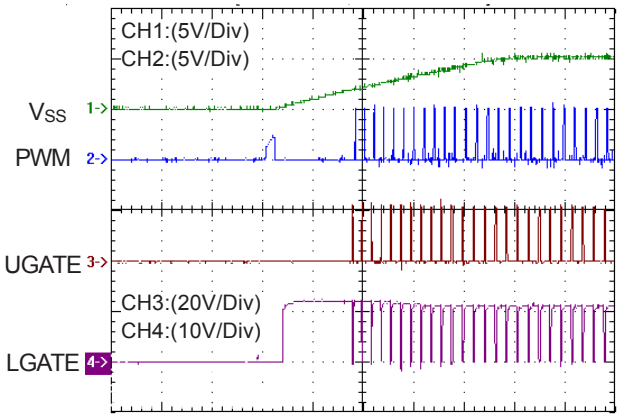
Time (25ms/Div)

Power-Off @ I_{OUT} = 60A



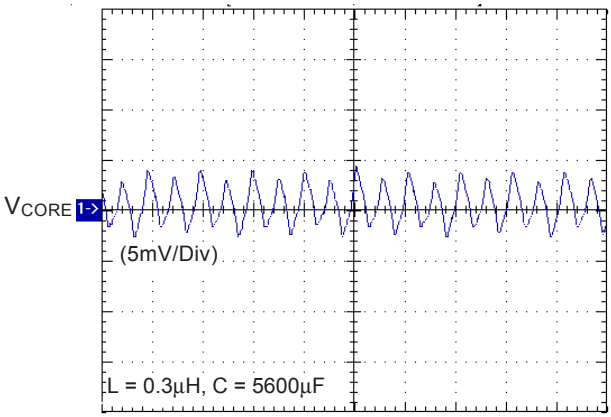
Time (10µs/Div)

Power-On @ I_{OUT} = 60A



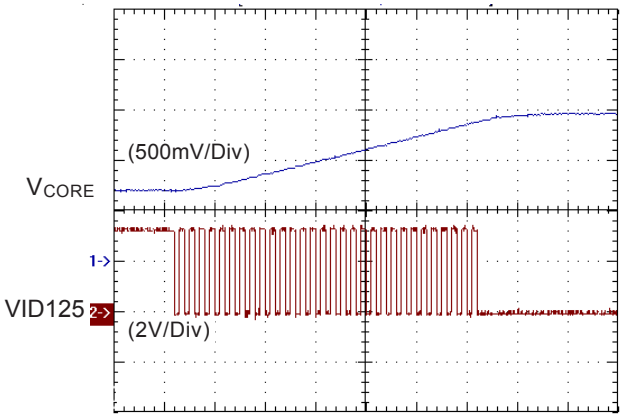
Time (10ms/Div)

Ripple



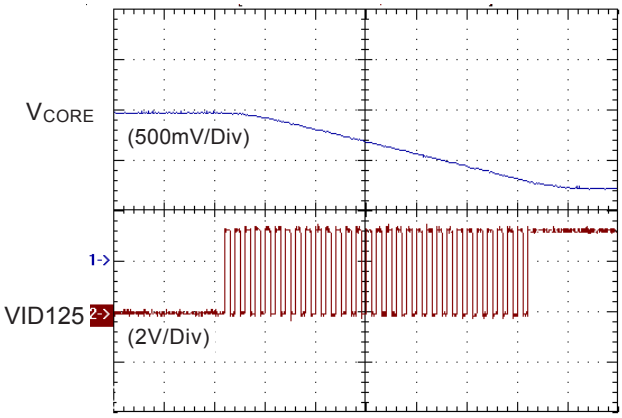
Time (2.5µs/Div)

DVID at Rising



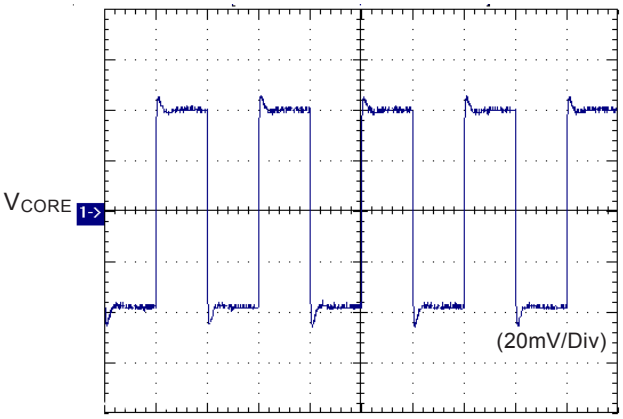
Time (50µs/Div)

DVID at Falling



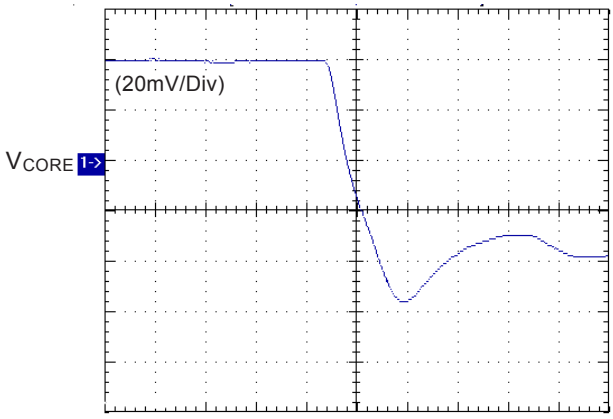
Time (50µs/Div)

Transient Response



Time (5ms/Div)

Transient Falling



Time (500ns/Div)

Application Information

RT9245A is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consisting of RT9245A and its companion MOSFET driver RT9619 provides high quality CPU power and all protection functions to meet the requirement of modern VRM.

Voltage Control

RT9245A senses the CPU V_{CORE} by SGND pin to sense the return of CPU to minimize the voltage drop on PCB trace at heavy load. OVP is sensed at FB pin. The internal high accuracy VID DAC provides the reference voltage for VRD10.x compliance. Control loop consists of error amplifier, multi-phase pulse width modulator, driver and power components. As conventional voltage mode PWM controller, the output voltage is locked at the V_{REF} of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase sawtooth wave. Power stage transforms VIN to output by PWM signal on-time ratio.

Current Balance

RT9245A senses the inductor current via inductor's DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal balance circuit.

The current balance circuit sums and averages the current signals and then produces the balancing signals injected to pulse width modulator. If the current of some power channel is larger than average, the balancing signal reduces that channels pulse width to keep current balance. The use of single GM amplifier via time sharing technique to sense all inductor currents can reduce the offset errors and linearity variation between GMs. Thus it can greatly improve signal processing especially when dealing with such small signal as voltage drop across DCR.

Droop & Load Line Setting

RT9245A injects averaged current $\overline{I_X}$ into the resistor R_{ADJ} connected to ADJ pin to generate a load-current-dependent voltage R_{ADJ} for droop setting :

$$V_{ADJ} = 8 \times \overline{I_X} \times R_{ADJ}$$

V_{ADJ} is then subtracted from VID_DAC output as the real reference voltage at non-inverting input of the error amplifier as shown if Figure 1. Consequently, load line slope is calculated as :

$$\text{Load Line} = \frac{\Delta V_{CORE}}{\Delta I_{CORE}} = \frac{8 \times R_{ADJ} \times DCR}{N \times R_{CSN}}$$

where N is the phase number of operation.

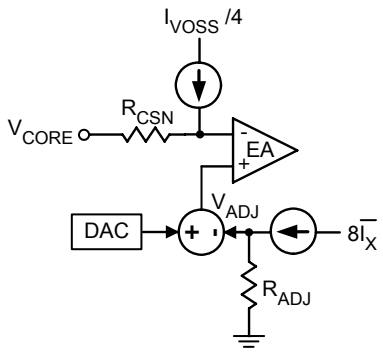


Figure 1. Load Line and Offset Function

Fault Detection

The chip detects FB for over voltage and power good detection. The “hiccup mode” operation of over current protection is adopted to reduce the short circuit current. The in-rush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

Phase Setting and Converter Start Up

RT9245A interfaces with companion MOSFET drivers (like RT9619, RT9607 series) for correct converter initialization. The tri-state PWM output (high, low and high impedance) senses its interface voltage when IC POR acts (both VCC and DVD trip). The channel is enabled if the pin voltage is 1.2V less than VCC. Tie the PWM to VCC and the corresponding current sense pins to GND or left float if the channel is unused. For example, for 3-Channel application, connect PWM4 high.

Current Sensing Setting

RT9245A senses the current flowing through inductor via its DCR for channel current balance and droop tuning.

The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal circuit (see Figure 2).

$$\frac{L}{DCR} = R \times C \quad V_C = DCR \times I_L \quad I_X = \frac{V_C}{R_{CSN}}$$

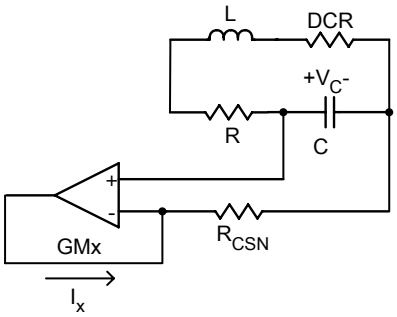


Figure 2. Current Sense Circuit

Figure 3 is the test circuit for GM. We apply test signal at GM inputs and observe its signal process output at ADJ pin. Figure 4 shows the variation of signal processing of all channels. We observe zero offsets and good linearity between phases.

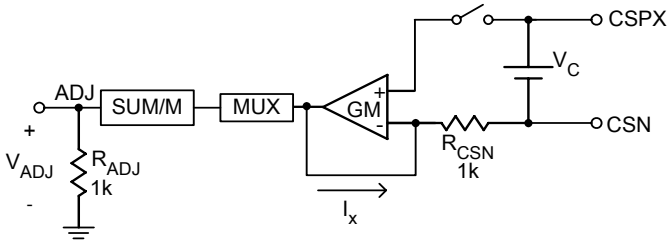


Figure 3. The Test Circuit of GM

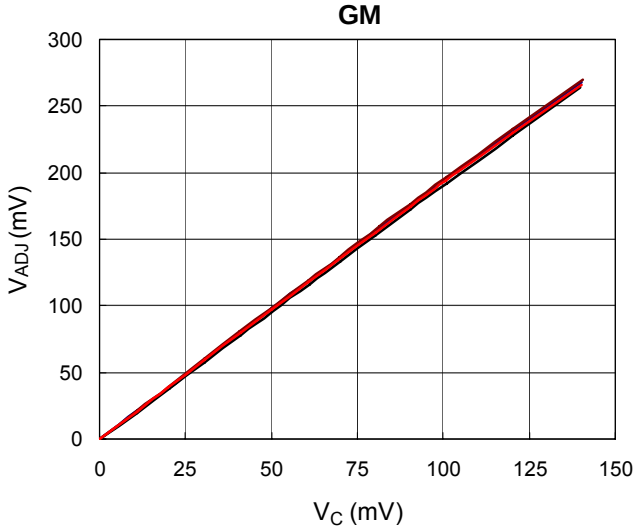


Figure 4. The Linearity of GMx

Figure 5 shows the time sharing technique of GM amplifier. We apply test signal at phase 4 and observe the waveforms at both pins of GM amplifier. The waveforms show time sharing mechanism and the perfomance of GM to hold both input pins equal when the shared time is on.

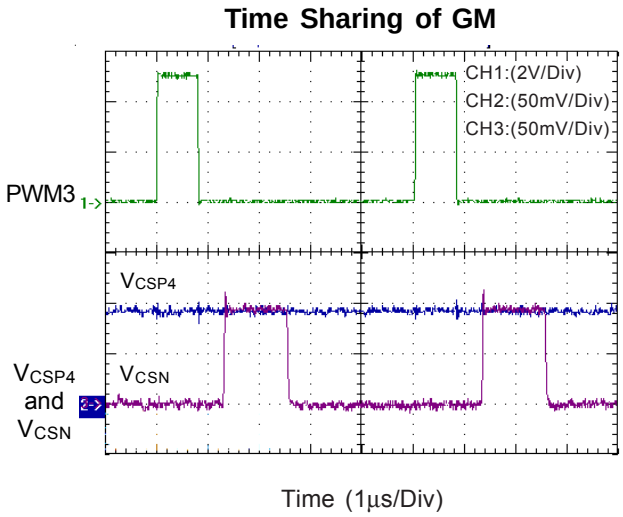


Figure 5

Over Current Protection

RT9245A uses an external resistor R_{IMAX} to set a programmable over current trip point. OCP comparator compares each inductor current with this reference current. RT9245A uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground.

$$\frac{1}{2} \times \frac{V_{IMAX}}{R_{IMAX}} \Leftrightarrow \frac{1}{3} \times \frac{I_L \times DCR}{R_{CSN}}$$

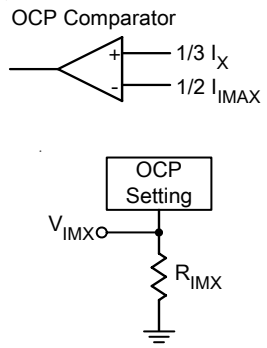


Figure 6. Over Current Comparator

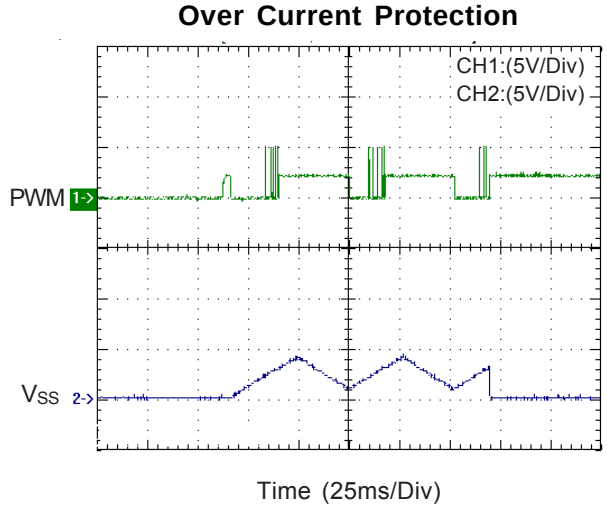


Figure 7. The Over Current Protection in the soft start interval

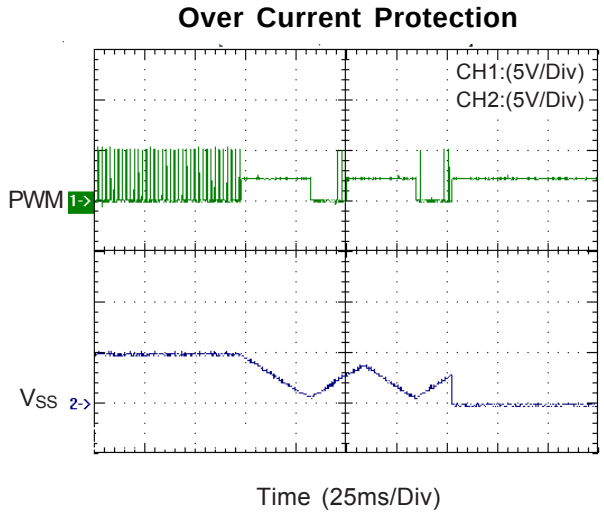


Figure 8. Over Current Protection at steady state

Current Ratio Setting

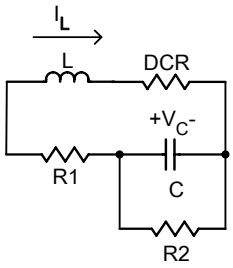


Figure 9. Application circuit for current ratio setting

For some case with preferable current ratio instead of current balance, the corresponding technique is provided. Due to different physical environment of each channel, it is necessary to slightly adjust current loading between channels. Figure 9 shows the application circuit of GM for current ratio requirement. Applying KVL along L+DCR branch and R1+C//R2 branch :

$$L\frac{dI_L}{dt}+DCR\times I_L=R_1(\frac{V_C}{R_2}+C\frac{dV_C}{dt})+V_C$$

$$=R_1C\frac{dV_C}{dt}+\frac{R_1+R_2}{R_2}V_C$$

$$\text{For}\quad V_C=\frac{R2}{R_1+R_2}DCR\times I_L$$

Look for its corresponding conditions :

$$L\frac{dI_L}{dt}+DCR\times I_L=(R1//R2)\times C\times DCR\times\frac{dI_L}{dt}+DCR\times I_L$$

$$\text{Let}\quad \frac{L}{DCR}=(R1//R2)\times C$$

$$\text{Thus if}\quad \frac{L}{DCR}=(R1//R2)\times C$$

$$\text{Then}\quad V_C=\frac{R2}{R1+R2}\times DCR\times I_L$$

With internal current balance function, this phase would share $(R_1+R_2)/R_2$ times current than other phases. Figure 10 & 11 show different settings for the power stages. Figure 12 shows the performance of current ratio compared with conventional current balance function in Figure 13.

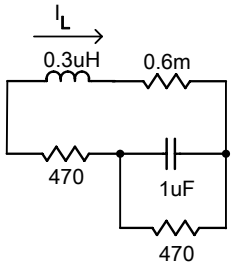


Figure 10. GM4 Setting for current ratio function

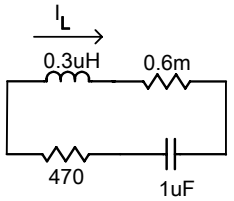


Figure 11. GM1~3 Setting for current ratio function

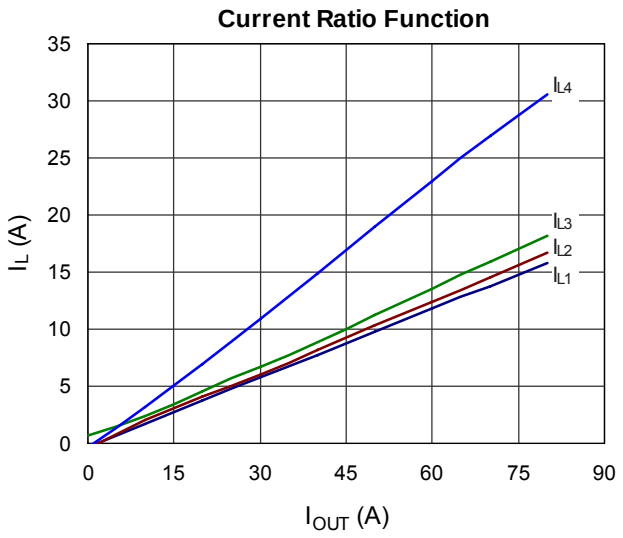


Figure 12

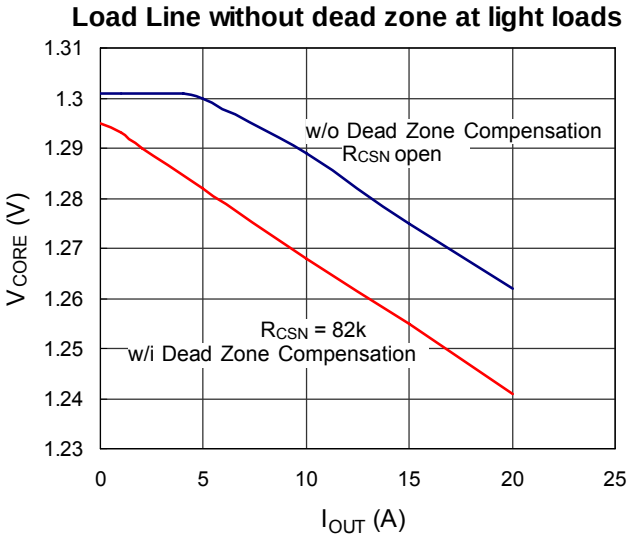


Figure 14

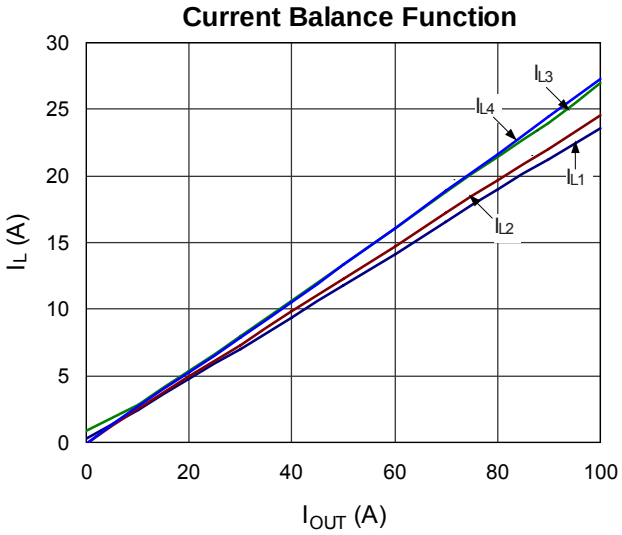


Figure 13

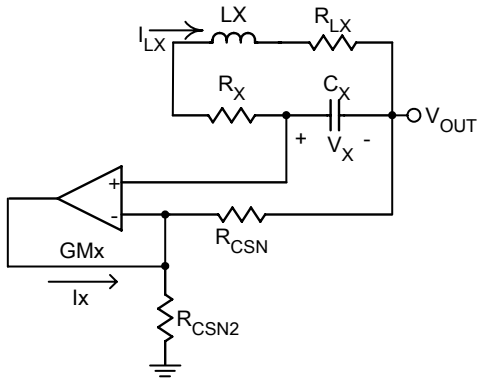


Figure 15. Application circuit of GM

Dead Zone Elimination

RT9245A samples and holds inductor current at 50% period by time-sharing sourcing a current I_X to R_{CSN}. At light load condition when inductor current is not balance, voltage V_X across the sensing capacitor would be negative. It needs a negative I_X to sense the voltage. However, RT9245A CANNOT provide a negative I_X and consequently cannot sense negative inductor current. This results in dead zone of load line performance as shown in Figure 14. Therefore a technique as shown in Figure 15 is required to eliminate the dead zone of load line at light load condition.

Referring to Figure 15, I_X is expressed as :

$$I_X = \frac{V_{OUT}}{R_{CSN2}} + \frac{I_{LX\_50\%} \times R_{LX}}{R_{CSN2}} + \frac{I_{LX\_50\%} \times R_{LX}}{R_{CSN}} \quad (1)$$

where $I_{LX\_50\%}$ is the of inductor current at 50% period. To make sure RT9245A could sense the inductor current, right hand side of Equation (1) should always be positive:

$$\frac{V_{OUT}}{R_{CSN2}} + \frac{I_{LX\_50\%} \times R_{LX}}{R_{CSN2}} + \frac{I_{LX\_50\%} \times R_{LX}}{R_{CSN}} \geq 0 \quad (2)$$

Since $R_{CSN2} >> R_{CSN}$ in practical application, Equation (2) could be simplified as :

$$\frac{V_{OUT}}{R_{CSN2}} \geq \left| \frac{I_{LX\_50\%} \times R_{LX}}{R_{CSN}} \right|$$

Figure 14 shows that dead zone of load line at light load is eliminated by applying this technique.

VID on the Fly

With external pull up resistors tied to VID pins, RT9245A converters different VID codes from CPU into output voltage. Figure 16 and Figure 17 show the waveforms of VID on the fly function.

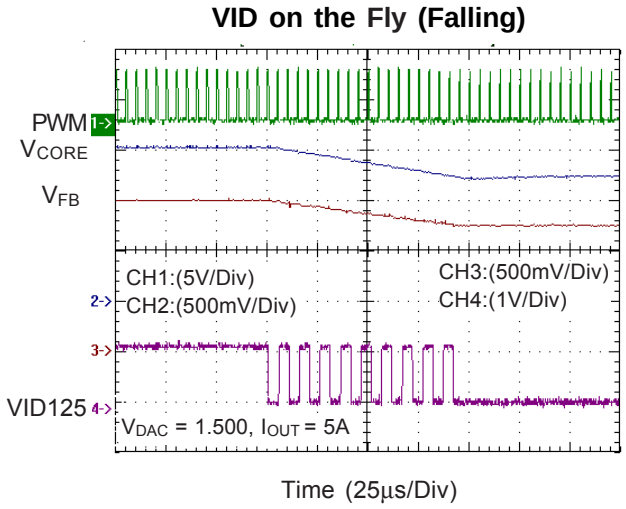


Figure 16

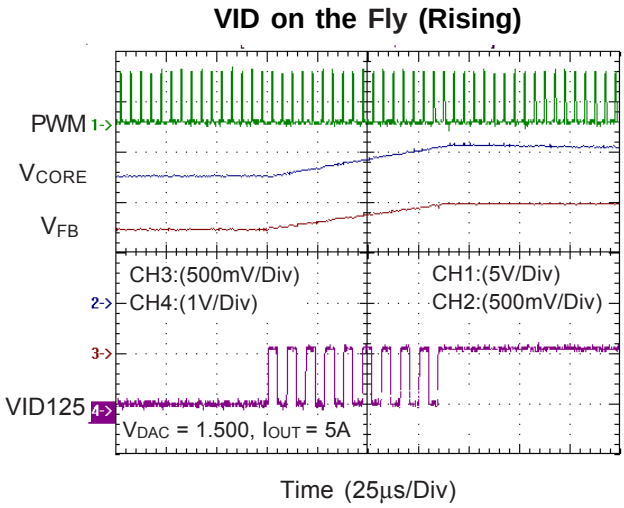


Figure 17

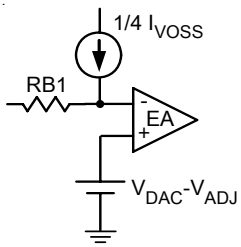


Figure 18. Offset Setting

Output Voltage Offset Function

To meet Intel® requirement of initial offset of load line, RT9245A provides programmable initial offset function. External resistor R_{VOSS} and voltage source at VOSS pin generate offset current $I_{VOSS} = \frac{V_{VOSS}}{R_{VOSS}}$, where V_{VOSS} is 1V typical. One quarter of I_{VOSS} flows through RB1 as shown in Figure 18. Error amplifier would hold the inverting pin equal to V_{DAC} - V_{ADJ}. Thus output voltage is subtracted from V_{DAC} - V_{ADJ} for a constant offset voltage.

$$V_{CORE} = V_{DAC} - V_{ADJ} - \frac{R_{FB1}}{4 \times R_{VOSS}}$$

A positive output voltage offset is possible by connecting R_{VOSS} to VDD instead of to GND. Please note that when R_{VOSS} is connected to VDD, V_{VOSS} is V_{DD} – 2V typically and half of I_{VOSS} flows through R_{FB1}. V_{CORE} is rewritten as:

$$V_{CORE} = V_{DAC} - V_{ADJ} + \frac{R_{FB1}}{R_{VOSS}}$$

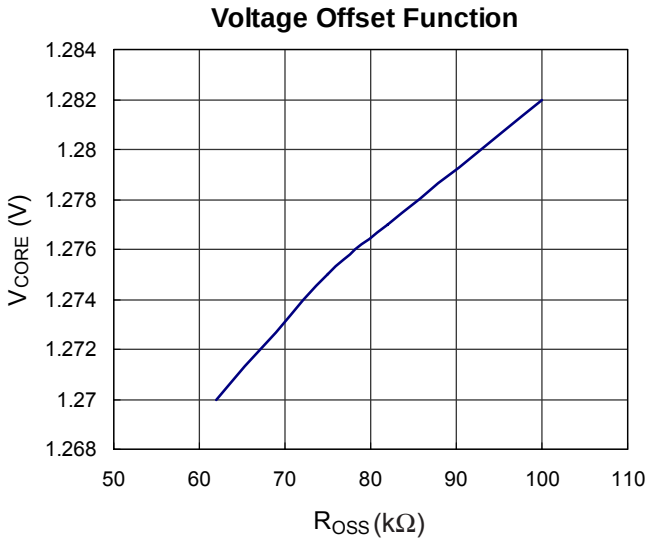


Figure 19

Load Line Setting and Thermal Compensation

V_{ADJ} = 8 x AVG(I_X) x R_{ADJ}

V_{OUT} = V_{DAC} - V_{ADJ}

AVG(I_X) is a PTC current. By properly use an NTC resistor at ADJ. Load line can be thermally compensated.

PGOOD Function

During start-up, RT9245A will detect $5V_{CC}$ and $12V_{IN}$ (through DVD pin). In Figure 21, $5V_{CC}$ or $12V_{IN}$ is not ready during T1. $V_{(SS)}$ (in Figure 20) is pulled to GND by FAULT. $V_{(EAP)}$ is also equal to GND. $V_{(FB)}$ and V_{OUT} will try to follow $V_{(EAP)}$ thus both $V_{(FB)}$ and V_{OUT} are equal to GND during T1. During T2, both $5V_{CC}$ and $12V_{IN}$ are ready, FAULT = low, OPSS starts charging up C_{SS}. In the design of RT9245A, I_{SS} (the maximal current sink and source capability of OPSS) is limited and time-variant. During T2 (V1 = 0.4V > $V_{(SS)}$ > 0), $I_{SS(T2)}$ is equal to about 10uA.

$$T2 = Css \times \frac{V1}{I_{SS(T2)}} \cong 4x10^4 \times Css$$

After $V_{(SS)}$ > V1, I_{SS} changes to about 20uA. The rising speed of $V_{(SS)}$ becomes about 2 times faster than in T1. In Figure 20, MOSFET N1 will turn on only if $V_{(SS)} > V_{TH\_N1}$ (threshold voltage of N1) ≅ 0.7V = V2. Before N1 turns on, $V_{(EAP)}$ is still 0V.

$$T3 = Css \times \frac{(V2 - V1)}{I_{SS(T3)}} \cong 1.5x10^4 \times Css$$

After $V_{(SS)}$ > V2, MOSFET N1 turns on, $V_{(EAP)}$ starts rising. I_{SS}(T4) is still equal to about 20uA. $V_{(SS,EAP)}$ is equal to V_{TH_N1}. Due to the body effect of MOSFET N1, V_{TH_N1} increases with higher $V_{(EAP)}$. For example, if V_{OUT} target is 1.4V, $V_{(SS,EAP)}$ will be equal to about 0.7V at the beginning of T4 and equal to about 1.1V at the end of T4.

$$T4 = Css \times \frac{(V4 - V2)}{I_{SS(T4)}} \cong 9x10^4 \times Css$$

At the end of T4, V_{OUT} is very close to the target (within the range of ±40mV). An internal 1ms timer starts. After about 1ms(T5), The open-drain output PGOOD releases.

After PGOOD releases, I_{SS}(T6) becomes about 320uA to accelerate OPSS. RT9245A enters normal operation mode and is capable to follow VID on the fly.

When any of the fault conditions happens, $V_{(SS)}$ and PGOOD will be pulled low immediately. If the fault condition is one of $5V_{CC}$ low, DVD low, OC or VID_OFF, RT9245A will try to turn off both high side MOSFET and low side MOSFET. V_{OUT} will fall slowly to avoid negative V_{OUT}. The typical waveform is shown in Figure 22.

If the fault condition is OV, $V_{(SS)}$ and PGOOD will be pulled low immediately also. RT9245A will try to turn on low side MOSFET and turn off high side MOSFET. V_{OUT} will fall quickly to protect CPU from high voltage. The typical waveform is shown in Figure 23.

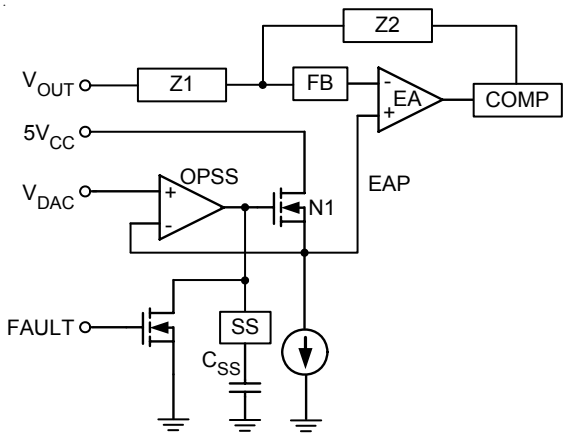


Figure 20. Soft Start Circuit

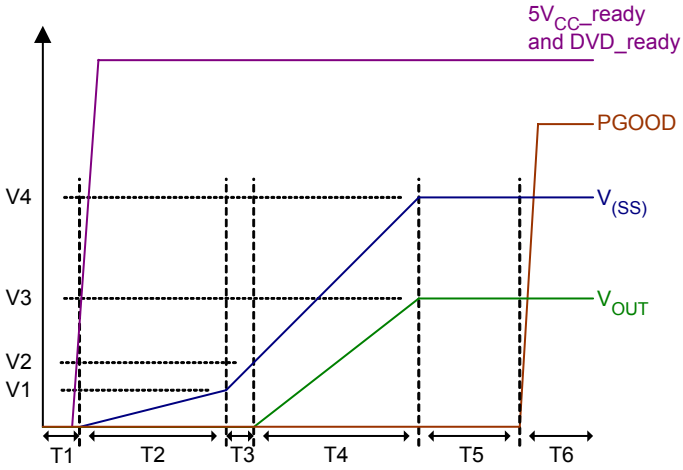


Figure 21. Soft Start Waveform

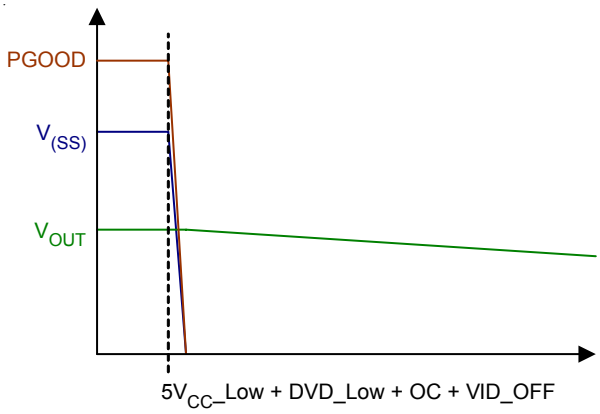


Figure 22. Waveform for $5V_{CC}$_Low, DVD_Low, OC or VID_OFF

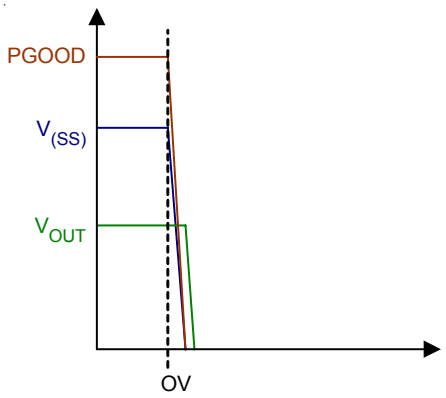


Figure 23. Waveform for OV

Error Amplifier Characteristic

For fast response of converter to meet stringent output current transient response, RT9245A provides large slew rate capability and high gain-bandwidth performance.

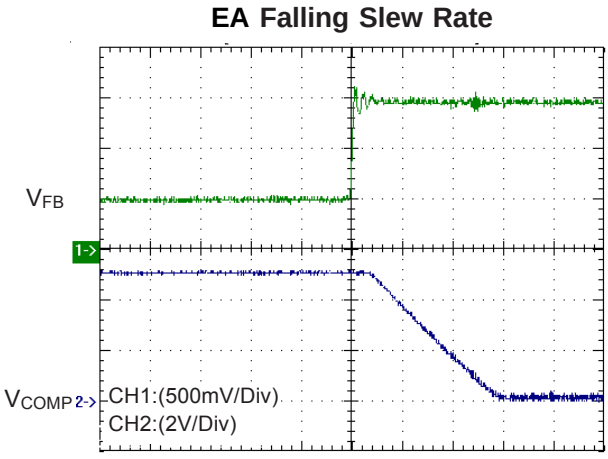


Figure 24. EA Rising Transient with 10pF Loading; Slew Rate = 8V/us

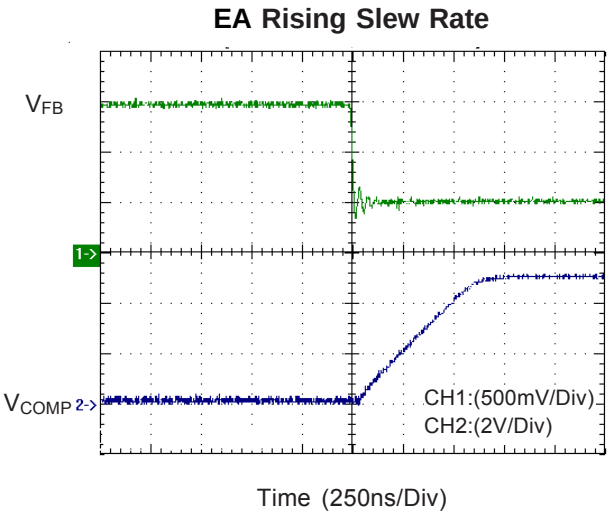


Figure 25. EA Falling Transient with 10pF Loading; Slew Rate = 8V/us

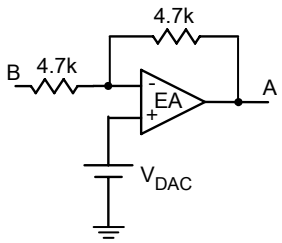


Figure 26. Gain-Bandwidth Measurement by signal A divided by signal B

Figure 27. EA Frequency Response with closed loop gain set at 0db to observe gain-bandwidth product; -3dB at 10.86MHz

Design Procedure Suggestion

a. Output filter pole and zero (Inductor, output capacitor value & ESR).

b. Error amplifier compensation & sawtooth wave amplitude (compensation network).

c. Kelvin sense for V_{CORE}.

Current Loop Setting

a. GM amplifier S/H current (current sense component DCR, CSN pin external resistor value).

b. Over-current protection trip point (R_{IMAX} resistor).

VRM Load Line Setting

a. Droop amplitude (ADJ pin resistor).

b. No load offset (R_{CSN2})

c. DAC offset voltage setting (VOSS pin & compen- sation network resistor RB1).

Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

a. Kelvin sense for current sense GM amplifier input.

b. Refer to layout guide for other items.

Voltage Loop Setting

Design Example

Given :

Apply for four phase converter

V_{IN} = 12V

V_{CORE} = 1.4V

I_{LOAD} = 30A to 125A

V_{DROOP} = 95mV with load (1mΩ Load Line)

OCP trip point set at 40A for each channel (S/H)

DCR = 1mΩ of inductor at 25°C

L = 0.3µH

C_{OUT} = 5600µF with 1mΩ equivalent ESR.

1. Compensation Setting

a. Modulator Gain, Pole and Zero :

From the following formula:

Modulator Gain = V_{IN}/V_{RAMP} = 12/1.9 = 6.3 (i.e 16dB)

where V_{RAMP} : Ramp amplitude of saw-tooth wave

LC Filter Pole = 3.88kHz and

ESR Zero = 28kHz

b. EA Compensation Network :

Select RB1 = 1.5k, RB2 = 15k, C1 = 2.7nF, C2 = 5.6pF, C3 = 680pF and use the Type 3 compensation scheme shown in Figure 28. By calculation.

$$F_{Z1} = \frac{1}{2p \times RB1 \times C3} = 156kHz$$

$$F_{Z2} = \frac{1}{2p \times RB2 \times C1} = 3.9kHz$$

$$F_P = \frac{1}{2p \times RB2 \times (C2//C1)} = 5.8kHz$$

Middle Band Gain = 10 (i.e. 20dB)

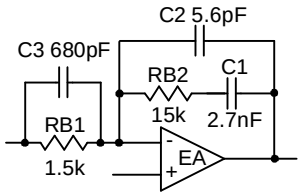


Figure 28. Type 3 compensation network of EA

The over all loop gain with load is shown in Figure 29 to Figure 31.

3. Over-Current Protection Setting

Consider the temperature coefficient of copper 3900ppm/°C,

$$\frac{1}{2} \times \frac{V_{IMAX}}{R_{IMAX}} \Leftrightarrow \frac{1}{3} \times \frac{I_L \times DCR}{R_{CSN}}$$

$$\frac{1}{2} \times \frac{1V}{R_{IMAX}} \Leftrightarrow \frac{1}{3} \times \frac{40A \times 1.39m\Omega}{330\Omega}$$

$$\Rightarrow R_{IMAX} = 8.9k\Omega$$

4. Soft-Start Capacitor Selection

For most application cases, 0.1µF is a good engineering value.

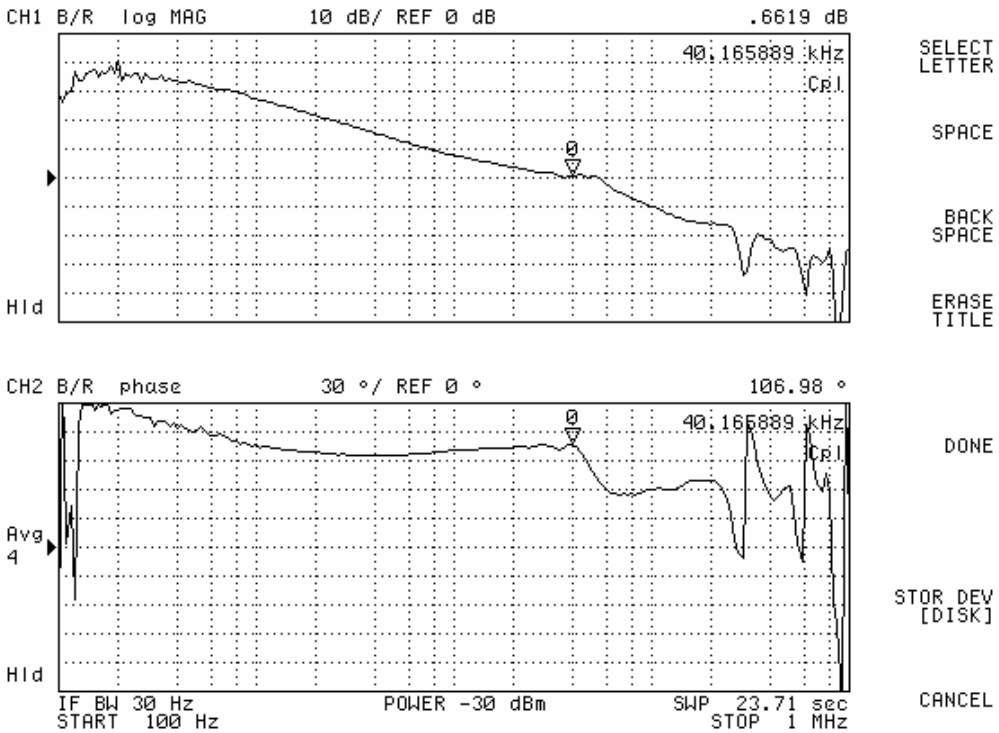


Figure 29. The Frequency Response with No Load

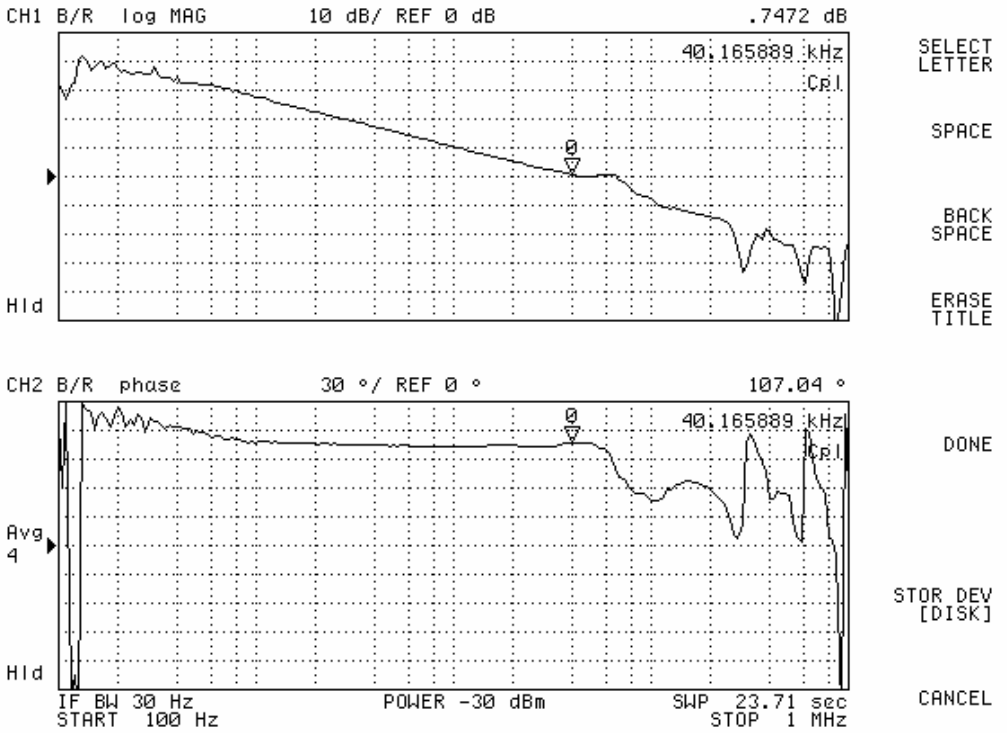


Figure 30. The Frequency Response with Middle Load

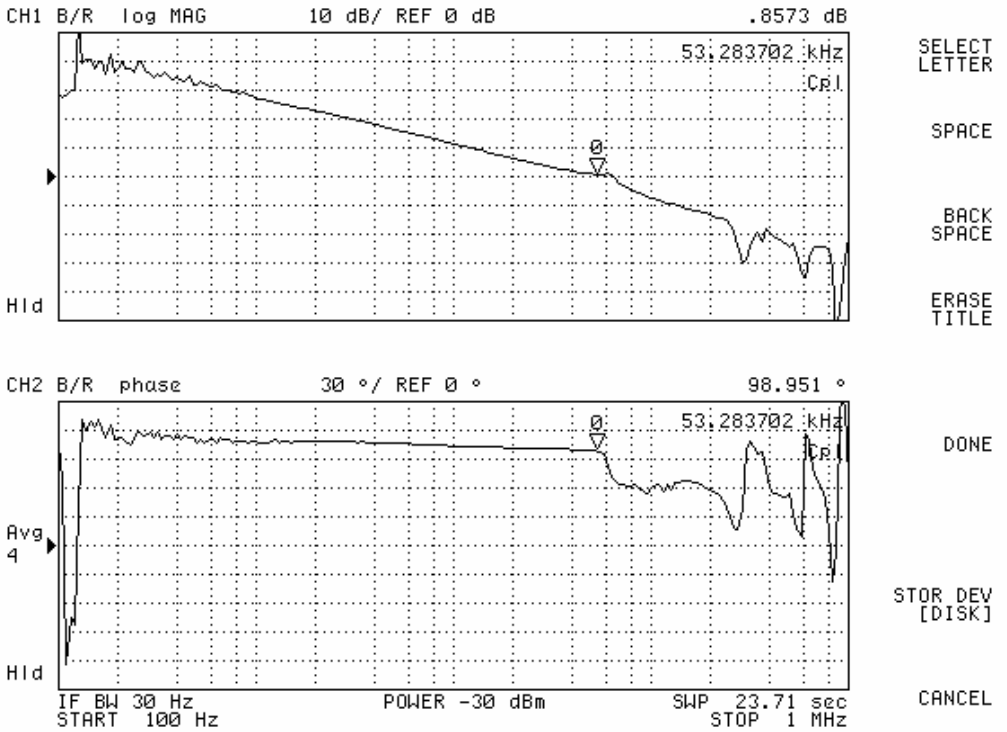


Figure 31. The Frequency Response with Heavy Load

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. **Most critical path: the current sense circuit is the most sensitive part of the converter. The current sense resistors tied to CSP1,2,3,4 and CSN should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible.**

2. Switching ripple current path:
   a. Input capacitor to high side MOSFET.
   b. Low side MOSFET to output capacitor.
   c. The return path of input and output capacitor.
   d. Separate the power and signal GND.
   e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.
   f. Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.

3. MOSFET driver should be closed to MOSFET.

4. The compensation, bypass and other function setting components should be near the IC and away from the noisy power path.

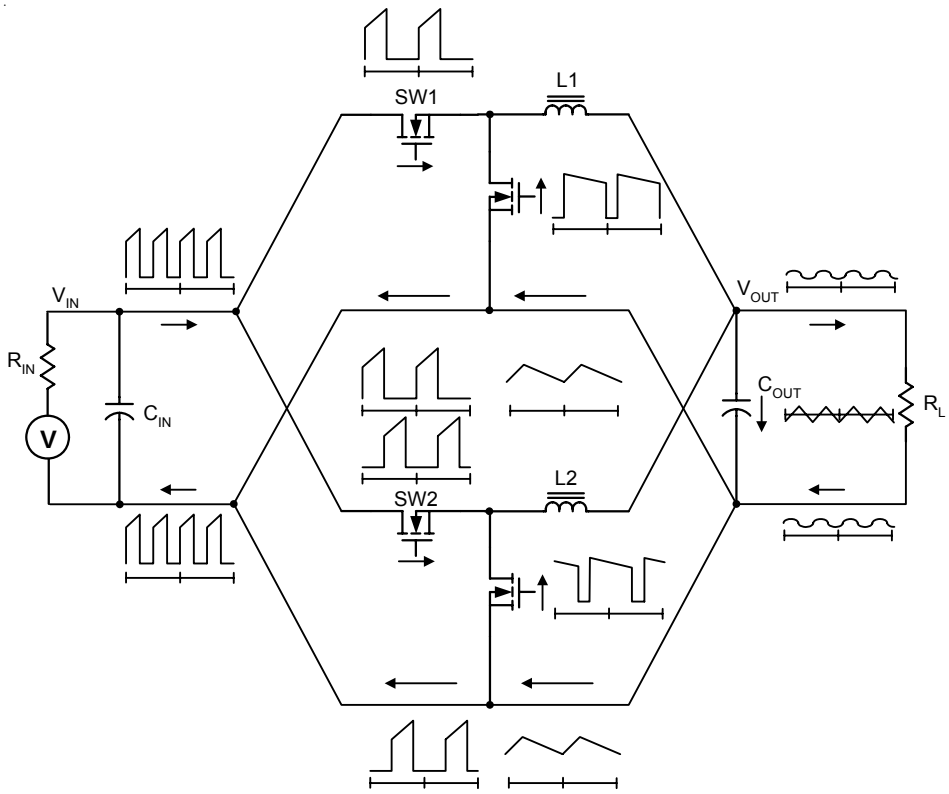


Figure 32. Power Stage Ripple Current Path

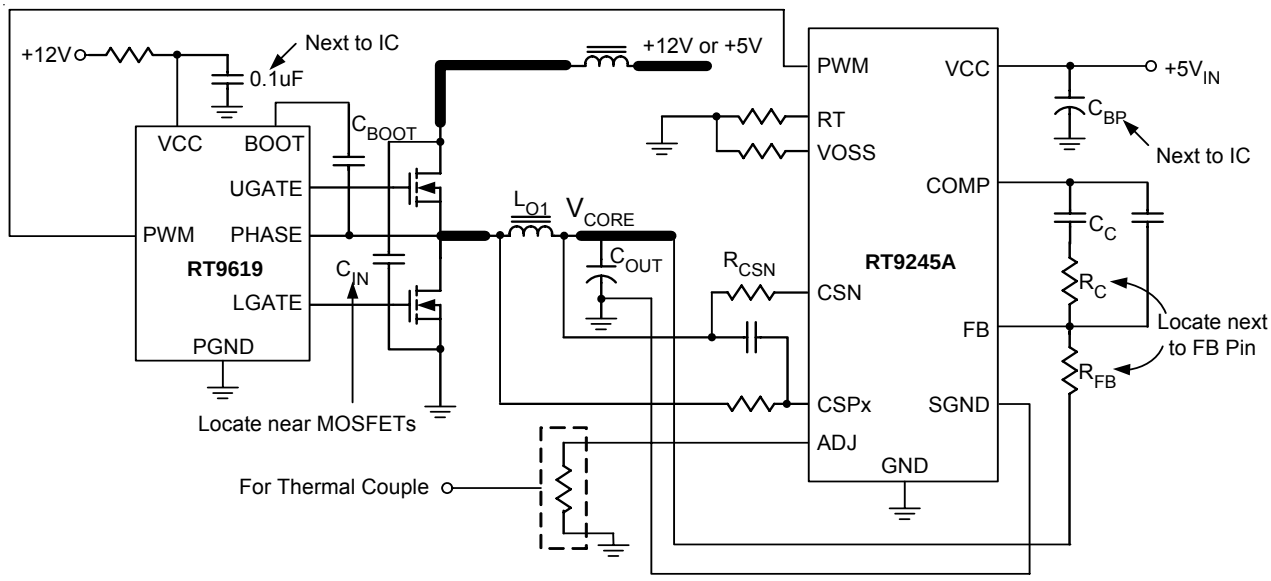


Figure 33. Layout Consideration

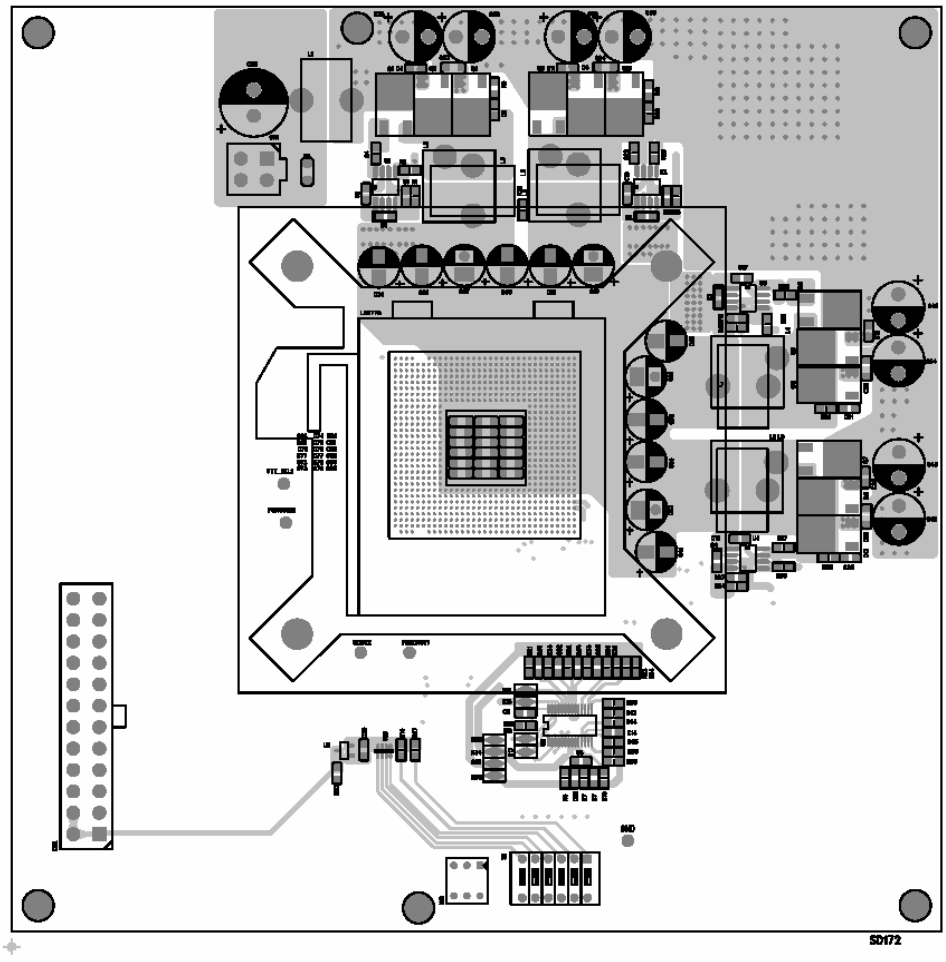
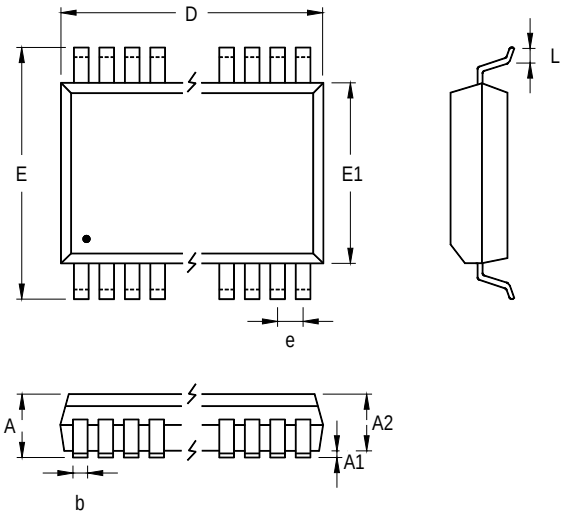


Figure 34. Layout of power stage

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.850	1.200	0.033	0.047
A1	0.050	0.152	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.178	0.305	0.007	0.012
D	9.601	9.804	0.378	0.386
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.293	4.496	0.169	0.177
L	0.450	0.762	0.018	0.030

28-Lead TSSOP Plastic Package

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